**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

1. (Currently Amended) A process for etching a low-k dielectric layer with selectivity to an overlying mask layer, comprising the steps of:

supporting a semiconductor substrate in a chamber of a plasma etch reactor, the semiconductor substrate having a low-k dielectric layer of a carbon-doped glass low-k material and an overlying mask layer;

supplying an oxygen-free single-fluorocarbon etching gas to the chamber and energizing the etching gas into a plasma state, the etching gas consisting essentially of at least one nitrogen reactant, ~~a single fluorocarbon reactant represented by $C_nF_m$ wherein n is at least 4 and m is at least 6~~ $C_5F_8$, and optional carrier gas, ~~the fluorocarbon reactant and nitrogen reactant being supplied to the chamber at flow rates such that the fluorocarbon reactant flow rate is less than the nitrogen reactant flow rate~~ wherein a flow ratio of $C_5F_8$ to the nitrogen reactant is 3 to 7%;

etching exposed portions of the low-k dielectric layer with the plasma so as to etch openings in the low-k dielectric layer with the plasma while providing a etch rate selectivity of the etching rate of the low-k dielectric layer to the etching rate of the mask layer of at least about 5, wherein the plasma etch reactor comprises a dual frequency parallel plate plasma reactor having a showerhead electrode and a bottom electrode on which the substrate is supported.

2. (Original) The process of claim 1, wherein the low-k dielectric layer is above an underlying silicon carbide layer, the etching rate of the low-k dielectric layer being at least 5 times faster than the etching rate of the silicon carbide layer.

3. (Original) The process of claim 1, wherein the low-k dielectric layer is above an underlying silicon nitride layer, the etching rate of the low-k dielectric layer being at least 5 times faster than the etching rate of the silicon nitride layer.

4. (Canceled)

5. (Canceled)

6. (Original) The process of claim 1, wherein the low-k dielectric layer overlies an electrically conductive or semiconductive layer comprising a metal-containing layer selected from the group consisting of doped and undoped polycrystalline or single crystal silicon, aluminum or alloy thereof, copper or alloy thereof, titanium or alloy thereof, tungsten or alloy thereof , molybdenum or alloy thereof, titanium nitride, titanium silicide, tungsten silicide, cobalt silicide, and molybdenum silicide.

7. (Original) The process of claim 1, wherein the openings are 0.25 micron or smaller sized openings.

8. (Canceled)

9. (Previously Presented) The process of claim 1, wherein the etching gas includes a carrier gas selected from the group consisting of Ar, He, Ne, Kr, Xe and mixtures thereof.

10. (Previously Presented) The process of claim 1, wherein the bottom electrode is supplied RF energy at two different frequencies or the showerhead electrode is supplied RF energy at a first frequency and the bottom electrode is supplied RF energy at a second frequency which is different than the first frequency.

11. (Canceled)

12. (Original) The process of claim 1, wherein the fluorocarbon reactant is supplied to the chamber at a flow rate of 3 to 30 sccm and the nitrogen reactant is supplied to the chamber at a flow rate of 50 to 300 sccm.

13. (Original) The process of claim 1, further comprising applying an RF bias to the semiconductor substrate during the etching step.

14. (Original) The process of claim 1, further comprising filling the openings with metal after the etching step.

15. (Original) The process of claim 1, wherein the etching step is carried out as part of a process of manufacturing a damascene structure.

16. (Original) The process of claim 1, further comprising steps of forming a photoresist layer above the mask layer, patterning the photoresist layer to form a plurality of the openings, etching through the mask, the etching step forming via or contact openings in the low-k dielectric layer at locations where the mask is etched through.

17. (Original) The process of claim 1, wherein the openings are formed with an aspect ratio of at least 5:1.

18. (Previously Presented) The process of claim 1, wherein the etching gas consists essentially of $C_5F_8$, $N_2$ and Ar.

19. (Original) The process of claim 1, wherein the plasma reactor is at a pressure of 50 to 500 mTorr during the etching step.

20. (Original) The process of claim 1, wherein the semiconductor substrate comprises a silicon wafer supported on a substrate support and the substrate support is maintained at a temperature of 20 to 50°C during the etching step.

21. (Previously Presented) The process of claim 1, wherein the mask layer comprises a silicon-containing film selected from the group consisting of a doped

oxide, undoped oxide, silicon nitride, silicon carbide, silicon oxynitride and combinations thereof.

22. (Currently Amended) A process for etching a low-k dielectric layer with selectivity to an overlying mask layer, comprising the steps of:

supporting a semiconductor substrate in a chamber of a plasma etch reactor, the semiconductor substrate having a low-k dielectric layer of a doped glass low-k material and an overlying mask layer of silicon carbide or silicon nitride;

supplying an oxygen-free etching gas to the chamber and energizing the etching gas into a plasma state, the etching gas consisting essentially of $C_4F_8$, $CF_2H_2$, $N_2$ and optionally Ar, the $C_4F_8$, $CF_2H_2$ and $N_2$ being supplied to the chamber at flow rates such that the total $C_4F_8$ and $CF_2H_2$ flow rate is 30% or less of the $N_2$ flow rate; and

etching exposed portions of the low-k dielectric layer with the plasma so as to etch openings in the low-k dielectric layer with the plasma while providing a etch rate selectivity of the etching rate of the low-k dielectric layer to the etching rate of the mask layer of at least about 5.

23. (Previously Presented) The process of claim 22, wherein the flow rate of the $CF_2H_2$ is less than or equal to the flow rate of the $C_4F_8$.

24. (Previously Presented) The process of claim 22, wherein the plasma etch reactor has a showerhead electrode and a bottom electrode on which the substrate is supported, the bottom electrode is supplied RF energy at two different

frequencies or the showerhead electrode is supplied RF energy at a first frequency and the bottom electrode is supplied RF energy at a second frequency which is different than the first frequency.

25. (Previously Presented) The process of claim 16, wherein etch rate selectivity of the etching rate of the low-k dielectric layer to the etching rate of the photoresist layer is at least about 5.

26. (Canceled)

27. (Previously Presented) The process of claim 1, wherein the openings have substantially straight walls.

28. (Previously Presented) The process of claim 22, wherein the doped glass low-k material is carbon-doped.